What is claimed is:

1. A sensor for detecting a clock signal transmitting in a transmission system, comprising:
   a converter for converting the clock signal to a TTL (Transistor Transistor Logic) signal; and
   a low-pass filter for transforming the TTL signal into a DC signal, in which the DC signal being a detecting signal;
   whereby, when the clock signal is shut down, the low-pass filter outputs a detecting signal with low potential DC level ; when the clock signal is normal, the low-pass filter outputs a detecting signal with high potential DC level.
2. The sensor according to claim 1, wherein said clock signal is converted to said converter via a capacitor.
3. The sensor according to claim 1, wherein said high potential is a positive potential and said low potential is a zero potential.
4. The sensor according to claim 1, wherein said converter is a LVPECL (Low Voltage Positive Emitter Coupling Logic), a LVCMOS (Low Voltage Complementary Metal Oxidization Semiconductor), a SSTL (Stub Series Terminated Logic) or a HSTL (High Speed Transmitter Logic) to LVTTL (Low Voltage Transistor Transistor Logic) converter.
5. The sensor according to claim 1, wherein said low-pass filter is composed of diodes and capacitors.
6. The sensor according to claim 1, wherein said detecting signal can

drive an illuminator or a sound device through a microprocessor to emit a warning signal.

7. A sensor for detecting a clock signal transmitting in a transmission system, comprising:

a converter for converting the clock signal to a TTL (Transistor Transistor Logic) signal;

a low-pass filter for transforming the TTL signal into a DC signal; and

an inverter for transforming said the level of the DC signal into a detecting signal;

whereby, when the clock signal is shut down, the inverter outputs a detecting signal with high potential ; when the clock signal is normal, the inverter outputs a detecting signal with low potential.

8. The sensor according to claim 7, wherein said high potential is a positive potential and said low potential is a zero potential.

9. The sensor according to claim 7, wherein said clock signal is converted to said converter via a capacitor.

10. The sensor according to claim 7, wherein said converter is a LVPECL (Low Voltage Positive Emitter Coupling Logic), a LVCMOS (Low Voltage Complementary Metal Oxidization Semiconductor), a SSTL (Stub Series Terminated Logic) or a HSTL (High Speed Transmitter Logic) to LVTTL (Low Voltage Transistor Transistor Logic) converter.

11. The sensor according to claim 7, wherein said low-pass filter is composed of diodes and capacitors.

12. The sensor according to claim 7, wherein said inverter comprises a transistor circuit which defines a cut-in potential; when a potential of said pulse signal is lower than said cut-in potential, said transistor is maintained at a cut-off state, and outputs a detecting signal with a positive potential; when a potential of said pulse signal is higher than said cut-in potential, said transistor is maintained at a cut-in state, and outputs a detecting signal with a zero potential.
13. The sensor according to claim 7, wherein said cut-in potential of said transistor is 0.6V.
14. The sensor according to claim 7, wherein said detecting signal can drive an illuminator or a sound device through a microprocessor to emit a warning signal.